FJM50 1T4RSDR

FJM50 SDR Software Defined Radio

FPGA IQ

23mm × 23mm

FJM50 200MHz 6GHz 52kHz 100MHz

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FPGA

- 1T4R SDR
- 200MHz 6GHz
- Low-IF
- DBF
-
- IQ
- FPGA
- SERDES
-
-

- 1T4R
- 200 MHz – 6GHz
- 52kHz~100MHz
- TDD FDD

FJM50 1T4RSDR

- ADC/DAC 16
  -
    - TX ≥2dBm
    - TX ≤-60dBm
    - TX ≥50dBc
    - TX 0dB~36dB
    - TX OIP3≥20dBm
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    - RX 30dB
    - RX ≥60dBc
    - ≤15dB
    - OIP3: ≥40dBm
- PLL
- 50MHz~200MHz
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FPGA **XC7K325T**

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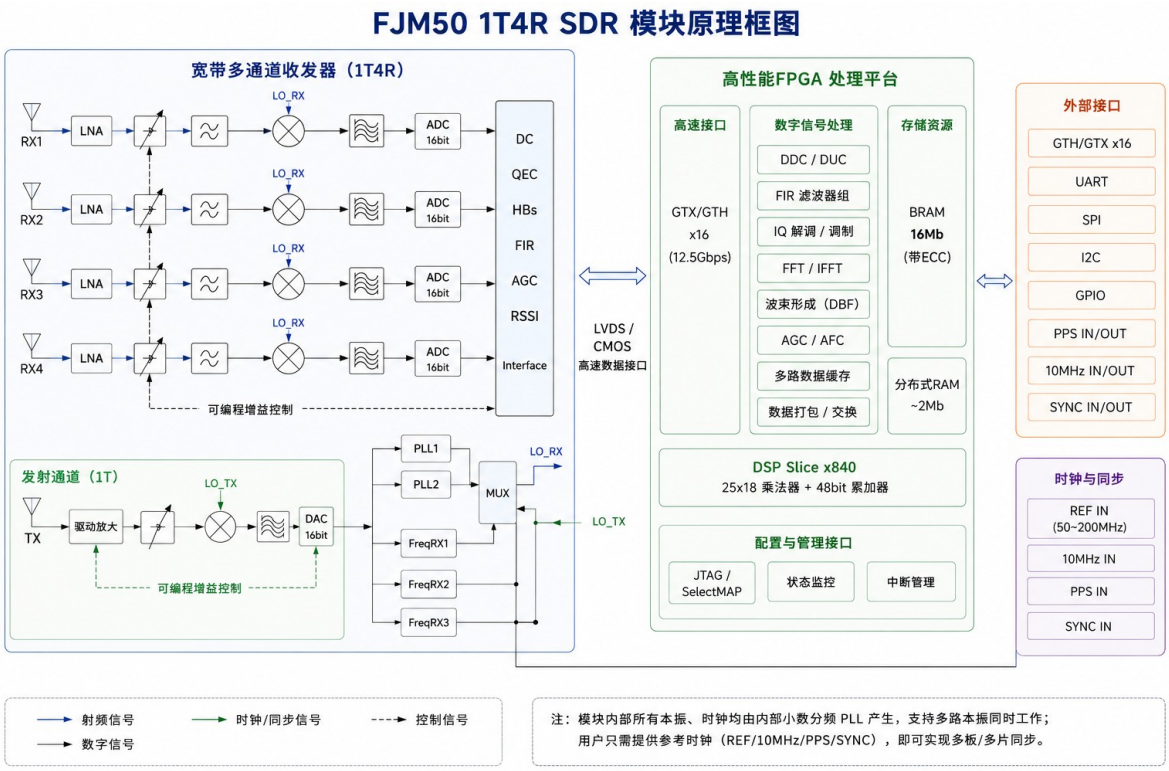
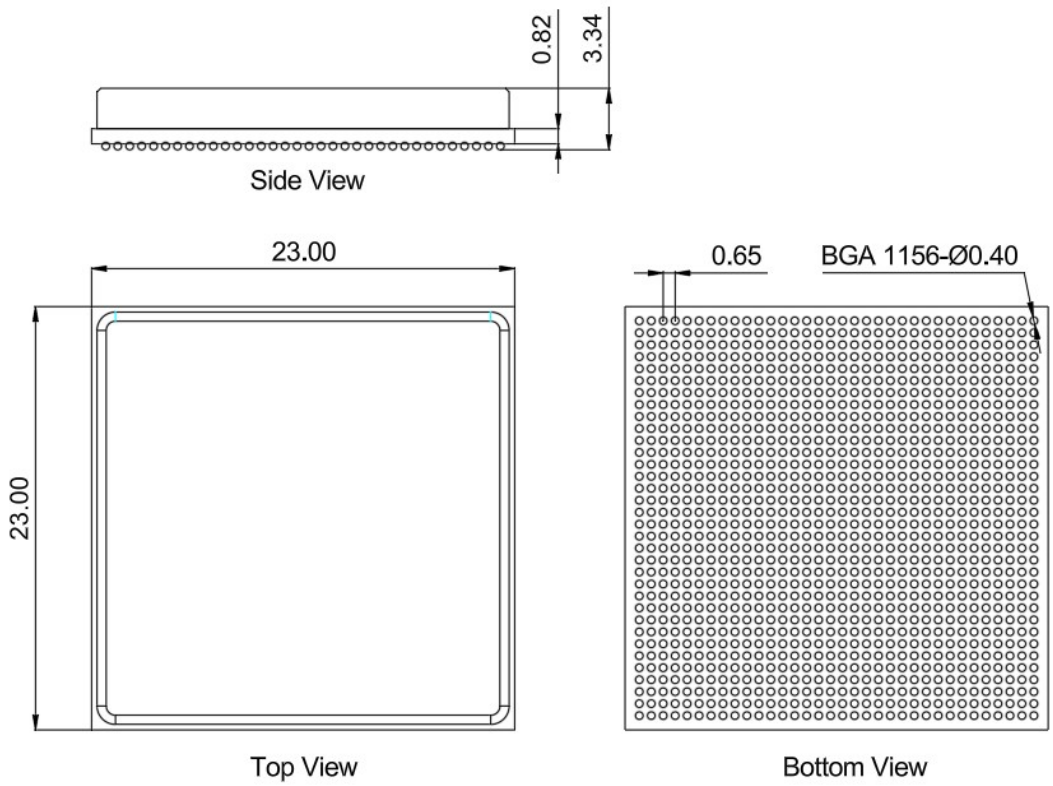
- Logic Cells 326,080
- LUT 6 203,800
- Flip-Flops 407,600
- CLB 25,475

- Block RAM BRAM 445 × 36 Kb 16,020 Kb 15.6 Mb
- RAM LUT RAM 2,000 Kb
- ECC 64 BRAM ECC

- DSP
  - DSP Slice 840
  - DSP 25×18 48
  - 2,845 GMAC/s
- GTH/GTX
  - 16
  - 12.5 Gb/s

FJM50 1T4RSDR





23×23×3.34mm

/ BGA/1156

650um

- BGA 400um