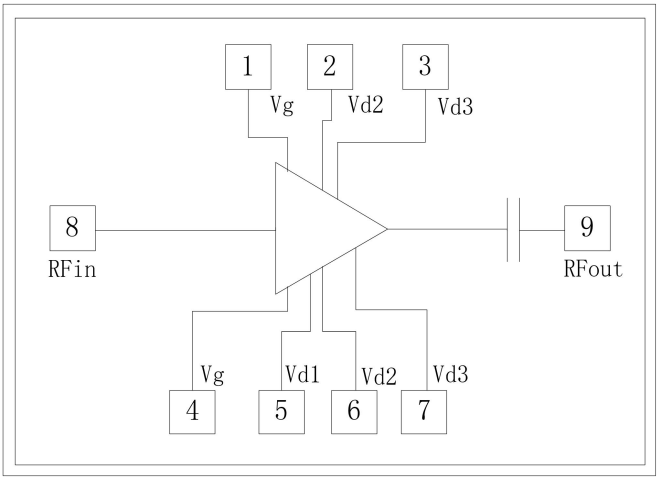
HYPA101
4~8GHz 120W GaN Power Amplifier

产品简介 Product Overview

HYPA101 chip is a high-performance 4-8 GHz high-power amplifiers, manufactured using a 0.25 μm gate length gallium nitride high electron mobility transistor (HEMT process). The chip is grounded through a back metal via a through-hole. The HYPA101 chip operates with dual power sources and can provide 51.5 dBm output power, 34 dB small signal gain and more than 32% power-added efficiency within 4-8 GHz with a drain voltage of Vds=48 V.

This chip is mainly used for transceiver components, wireless communication, etc.

功能框图 Functional Block Diagram



核心特性 Key Features

- 频率范围 Frequency Range: 4-8 GHz
- 功率附加效率 PAE: 32% (PIN=27 dBm, Pulsed)
- 输出功率 POUT: 51.5 dBm (PIN=27 dBm, Pulsed)
- 小信号增益 Small Signal Gain: 34 dB
- 输入电压驻波比 RFin VSWR: < 2.1
- 偏置条件 Bias: VD=48 V, IDQ=2.3 A
- 芯片尺寸 Chip Dimensions: 4.5 x 5.25 x 0.10 mm

订购信息 Ordering Information

型号 Part No.	描述 Description
HYPA101	4-8 GHz 120W GaN Power Amplifier

最大额定值 Absolute Maximum Ratings

参数额定值 Parameter Rating	
Drain Voltage (VD)	55
Gate Voltage Range (VG)	-5 V
Drain Current (ID)	11 A
Gate Current (IG)	----
Power Dissipation (P_{DISS}), 85 °C, PW=100 µs; DC=10 %	350 W
Input Power (P_{IN}) , 50 Ω, VD=28 V, 85 °C, Pulsed; PW=100 µs; DC=10%	33 dBm
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device.Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

推荐工作条件 Recommended Operating Conditions

参数 Parameter	Typ.	Units
Drain Voltage (VD)	48	V
Drain Current, Quiescent (IDQ)	2.3	A
Operating Temperature Range	−40 to 85	°C

Electrical specifications are measured at specified test conditions.Specifications are not guaranteed over all recommended operating conditions.

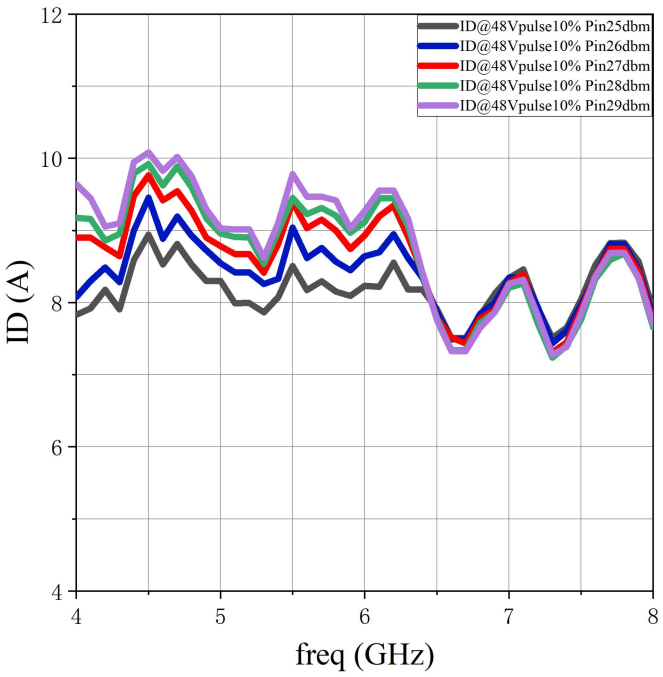
电气特性 Electrical Specificatios

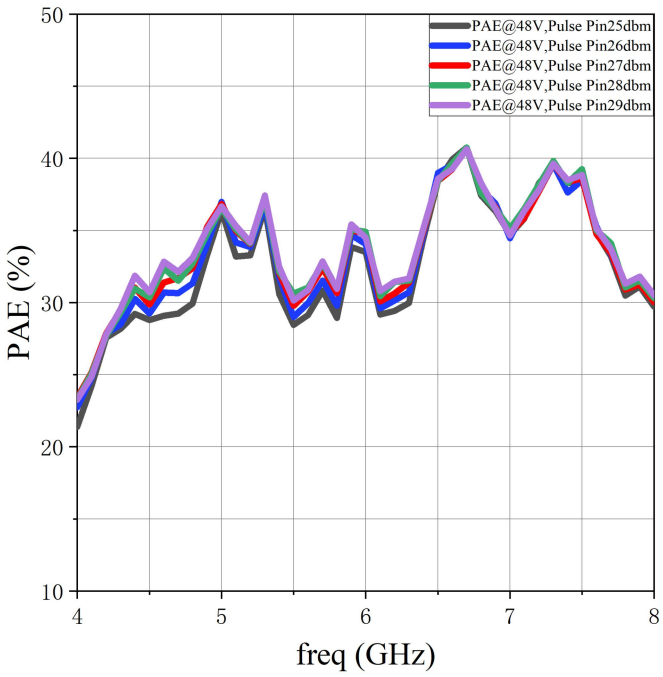
参数 Parameter	Min.	Typ.	Max.	Units
工作频率范围 Operational Frequency Range	4		8	GHz
输出功率 Output Power (Pin = 27 dBm)		51.5		dBm
功率附加效率 Power Added Efficiency (Pin = 27 dBm)		32		%
功率增益 Power Gain (Pin = 27 dBm)		24.5		dBm
小信号增益 Small Signal Gain		34		dBm
输入电压驻波比 RFin VSWR		2.0		
输出电压驻波比 Output VSWR		--		
小信号增益温度系数 Small Signal Gain Temperature Coefficient		-0.058		dB/°C
输出功率温度系数 Output Power Temperature Coefficient		-0.014		dBm/°C

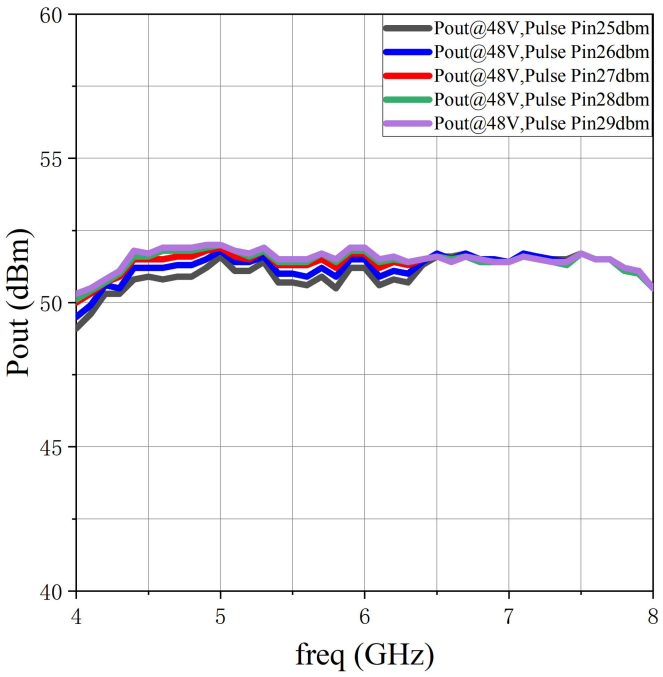
Test conditions unless otherwise noted: 25°C, VD=48 V, IDQ=2.3 A, P=100 µs, DC=10%

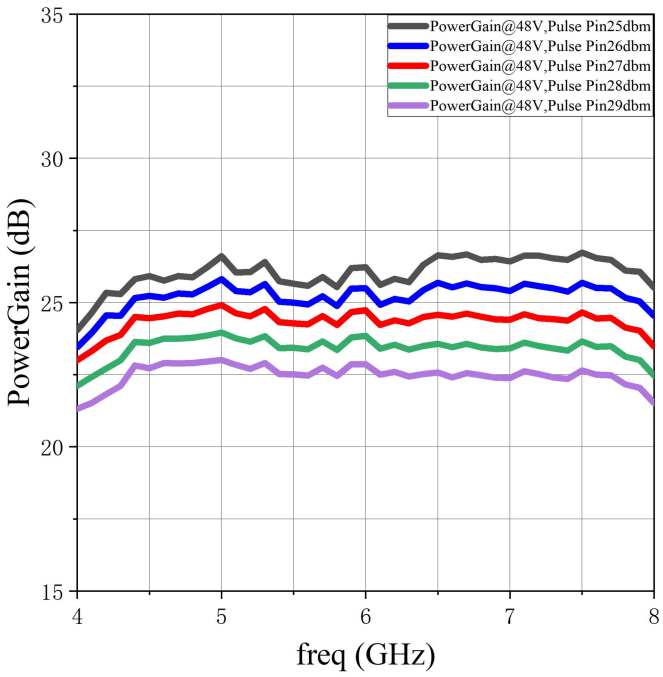
性能曲线 – 大信号（脉冲模式）Performance Plots – Large Signal (Pulsed)

测试条件 Test conditions: 25 °C, VD=48 V, IDQ=2.3 A, PIN=25-29 dBm, PW=100 µs, DC = 10%



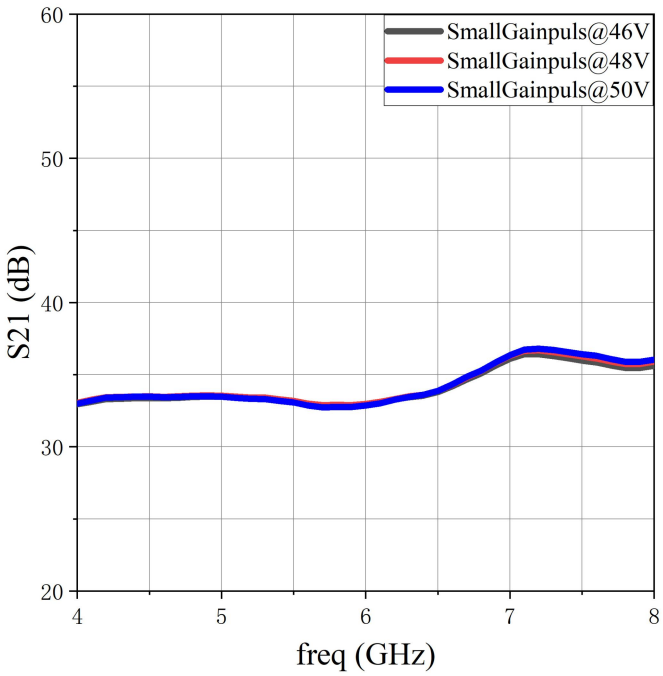


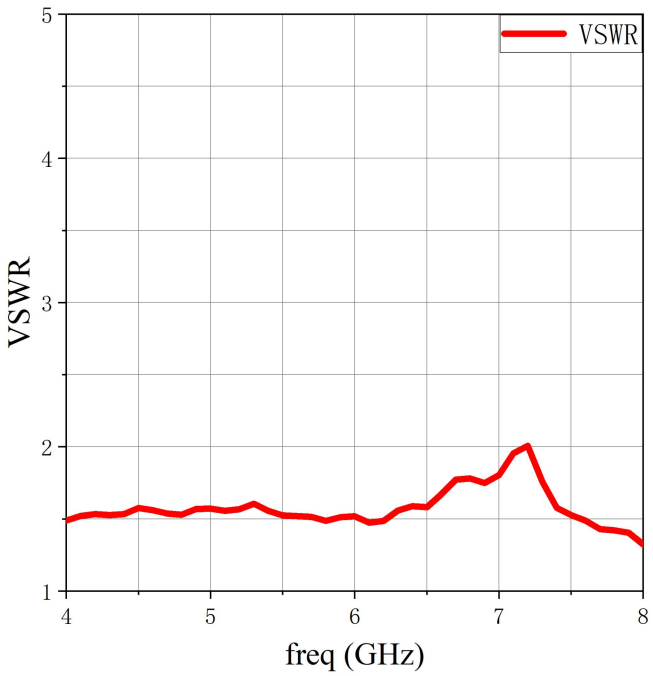




性能曲线 – 小信号（脉冲模式）Performance Plots – Small Signal (Pulsed)

测试条件 Test conditions: 25 °C, VD=46-50 V, IDQ=2.3 A, PIN=27 dBm, PW=100 µs, DC=10%

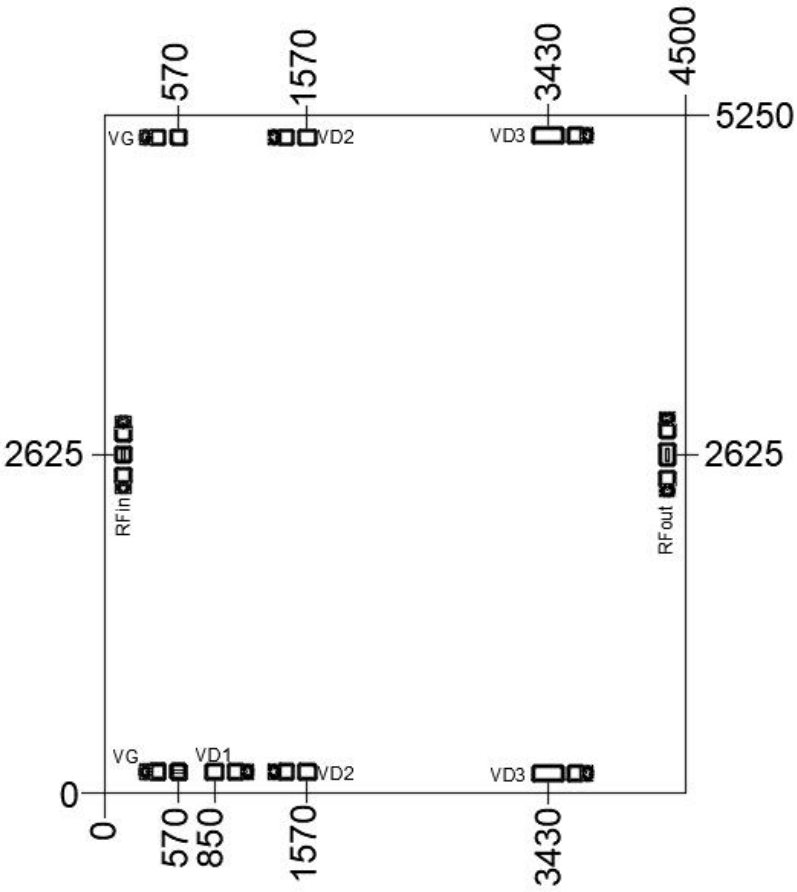




热阻参数信息 Thermal Resistance Information

参数 Parameter	测试条件 Test Conditions	数值 Value	单位 Units
Thermal Resistance	Tbase= 85 °C, Freq=5 GHz, Pulsed, VD=48 V,PIN=27 dBm, POUT = 51.8 dBm, ID_DRIVE=9.1 A, PDISS=280 W, PW=100 µs, DC=10%	0.24	°C/W
Channel Temperature		155	°C

芯片尺寸图及键合焊盘说明 Chip size diagram and Bond Pad Description

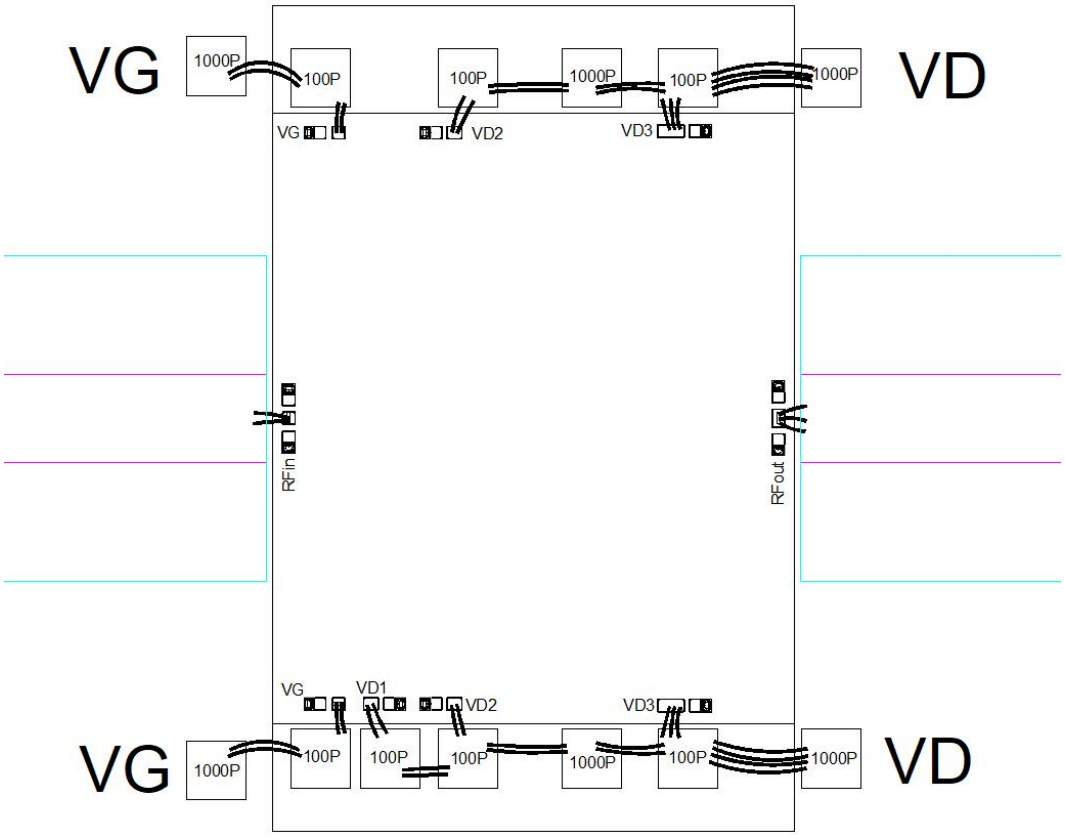


Units: μm
Thickness: 0.1 mm
Diex,y size tolerance: ± 0.050 mm
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

键合焊盘说明 Bond Pad Description

焊盘编号 Pad No.	焊盘标识 Symbol	焊盘尺寸（平方微米） Pad Size (μm²)	焊盘说明 Description
1,4	VG	110×110	Amplifier gate bias requires external 100pF and 1000pF capacitors.
5	VD1	130×110	Amplifier gate bias requires external 100pF and 1000pF capacitors. VD1 and VD2 and VD3 need to be connected across an external 1000pF capacitor.
2,6	VD2	130×110	
3,7	VD3	230×110	
8	RFin	110×110	RF signal input terminal, external 50 ohm system. If there is an external DC current at the voltage point, a DC isolation capacitor is required.
9	RFout	110×160	RF signal output terminal, external 50 ohm system, no need for DC isolation capacitor
Back of chip			The bottom of the chip needs to have good contact with RF and DC ground

芯片装配图 Chip Assembly Diagram



Notes: 1.VG & VD need to be biased from both sides.

偏置上电流程 Bias-Up Procedure

1. Set ID limit to 8000 mA, IG limit to 20 mA
2. Set VG to −5.0 V
4. Set VD +48 V
5. Adjust VG more positive until IDQ ≈ 2.3A
6. Apply RF signal

偏置下电流程 Bias-Down Procedure

1. Turn off RF signal
2. Reduce VG to −5.0 V. Ensure IDQ ~ 0 mA
4. Set VD to 0 V
5. Turn off VD supply
6. Turn off VG supply

装配注意事项Assembly Notes

Component placement and die attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Conductive epoxy attachment may be used for small-signal low power dissipation die.
- Follow manufacture instructions for epoxy curing.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized..
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermo sonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.